WHAT IS CLAIMED IS:

1. A vertical MOS transistor comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial growth layer of the first conductivity type which is formed on the semiconductor substrate;

a body region of a second conductivity type which is formed on the epitaxial growth layer;

a heavily doped body contact region of the second conductivity type which is formed on a part of a surface of the second conductivity type body region;

a heavily doped source region of the first conductivity type which is formed on a part of the surface of the second conductivity type body region that is not covered with the heavily doped body contact region;

a silicon trench piercing the second conductivity type body region and the first conductivity type source region to reach an inner part of the first conductivity type epitaxial growth layer;

a gate insulating film formed along walls and bottom of the silicon trench;

a heavily doped polycrystalline silicon gate buried in the silicon trench to a level of the first conductivity type source region while surrounded by the gate insulating film;

an intermediate insulating film formed on the polycrystalline silicon gate in the silicon trench to reach a surface of the

semiconductor substrate;

a metallic source electrode having a flat surface to be in contact with the intermediate insulating film, the heavily doped source region, and the heavily doped body contact region; and

a metallic drain electrode connected to a rear surface of the semiconductor substrate.

2. A vertical MOS transistor according to claim 1, wherein an insulator is provided on the side walls of the silicon trench above the heavily doped polycrystalline silicon gate.

3. A vertical MOS transistor according to claim 2, wherein the insulator provided on the side walls of the silicon trench is a silicon nitride film.

4. A vertical MOS transistor according to claim 3, wherein the heavily doped polycrystalline silicon gate buried in the silicon trench is 0.5 μm to 1.0 μm down from the top of the trench.

5. A vertical MOS transistor according to claim 2, wherein the heavily doped polycrystalline silicon gate buried in the silicon trench is 0.5 μm to 1.0 μm down from the top of the trench.

6. A vertical MOS transistor according to claim 1, wherein the heavily doped polycrystalline silicon gate buried in the silicon trench is 0.5 μm to 1.0 μm down from the top of the trench.